IN THE SPECIFICATION:

Please rewrite the previously-amended paragraph beginning at page 6, line 1, so that it reads as follows:

To create as large an efficient illuminating area as possible, it is the object of the present invention to make the opening region 81 an integral shape. Assuming the TFTs and capacitor regions 71, 72, and 73 are constant, the available area of the indium tin oxide region 8 is fixed. According to the geometry and the previously mentioned assumption, assuming the width W is fixed and the indium tin oxide region 8 is rectangular without being concave, the area of the indium tin oxide region 8 increases if the perimeter decreases (maximum area and minimum perimeter occur while the indium tin oxide region 8 is square). Therefore, the present invention makes the indium tin oxide region 8 an integral rectangle without being concave by arranging the TFTs and capacitor regions 71, 72, and 73 in a hoof shape to increase the efficient illuminating area. ~~Specifically, as shown in Fig. 3a, the rectangular pixel unit 3 has a first length L1 and a first width W1, and the rectangular opening region 81 has a second length L2 and a second width W2, wherein (L1 – L2) / (W1 – W2) > 1.~~ Opposite to the irregular arrangement of the conventional pixel unit layout mentioned above, the present invention improves the illuminating efficiency of the display with high aperture ratio.

Please rewrite the previously-amended paragraph beginning at page 7, line 2, so that it reads as follows:

FIG. 3b is a top view of a pixel unit in accordance with the second embodiment of the present invention. As shown in FIG. 3b, a pixel unit 3 is provided with a first thin film transistor region 71', a capacitor region 72', a second thin film transistor region 73' and an indium tin oxide region 8 (transparent region). To make the indium tin oxide region 8 an integral rectangle, the TFTs and capacitor regions 71', 72', and 73' are arranged in an L shape. According to this embodiment, the first thin film transistor region 71', capacitor region 72' and second thin film transistor region 73' are respectively disposed at the left side and bottom side. Thus, the indium tin oxide region 8

forms an integral rectangle such that the area of the opening region 81 increases. ~~As shown in Fig. 3b, the rectangular pixel unit 3 has a first length L1 and a first width W1, and the rectangular opening region 81 has a second length L2 and a second width W2, wherein (L1 – L2) / (W1 – W2) > 1.~~